Real Time Clock Module

Model RTC-58321

Features

Built-in crystal oscillator

- eliminates need for external components
- eliminates design time
- reduces board space

Low current consumption

Low-voltage battery backup function

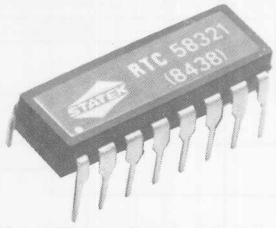
4-bit bidirectional multiplexed address/data bus

Counter start, stop and reset functions

12 or 24 hour format, automatic leap year selection

Interrupt signal outputs: 1024, 1, $\frac{1}{60}$, $\frac{1}{3600}$ Hz

Standard 16-pin DIP, pin-compatible with MSM 58321RS



Description

The RTC-58321 Real Time Clock Module incorporates a CMOS real time clock and a complete crystal oscillator in a standard 16-pin DIP. The combination of the real time clock and crystal oscillator in one package eliminates the need for an external crystal, resistors, and capacitors, resulting in a substantial reduction in design time and board space, as well as procurement, inventory, testing, and assembly costs. Application note available upon request.

Electrical Characteristics

Operating Ranges

Item	Symbol	Conditions	Range	Units
Supply voltage	V_{DD}	———	4.5~5.5	V
Data-holding voltage[1]	V_{DH}	———	2.2~5.5	V
Crystal frequency	f_o	———	32.768	kHz
Operating temperature	T_{OP}	———	−10~+60	℃

[1]Guarantees continued clock operation only.

Absolute Maximum Ratings

Item	Symbol	Conditions	Rated Value	Units
Supply voltage	V_{DD}	Ta=25℃	−0.3~7	V
Input voltage	V_I	Ta=25℃	GND−0.3~V_{DD}+0.3	V
Output voltage	V_o	Ta=25℃	GND−0.3~V_{DD}+0.3	V
Storage temperature	Tstg	———	−30~+80	℃

Electrical Characteristics

V_{DD}=5V±5% Ta=−10~+60℃

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
H. input voltage[1,2]	V_{IH1}	——	3.6	——	——	V
	V_{IH2}	——	V_{DD}−0.5	——	——	V
L. input voltage	V_{IL}	——	——	——	0.8	V
L. output voltage	V_{OL}	I_o=1.6mA	——	——	0.4	V
L. output current	I_{OL}	V_o=0.4V	1.6	——	——	mA
H. input current[3]	I_{IH}	V_I=5V	10	30	80	μA
L. input current[3]	I_{IL}	V_I=0V	——	——	−1	μA
D_0~D_3 terminals input off-leak current	I_{LIH}/I_{LIL}	V_I=5V V_I=0V	——	——	1 −1	μA
Input capacity	C_I	f=1MHz	——	5	——	pF
Current consumption	I_{OP}	Ta=25℃ V_{DD}=5V/V_{DD}=3V	——	16.5/6.2	30.0/10.0	μA
Accuracy[4]	△t/t	Ta=25℃ V_{DD}=5V	——	——	±4.5	sec/day

[1]CS2 WRITE, READ, ADDRESS-WRITE, STOP, TEST, D_0~D_3 terminals
[2]CS1 terminals
[3]CS1, CS2, WRITE, READ, ADDRESS-WRITE, STOP, TEST terminals
[4]Tighter accuracy available, contact factory
Specifications subject to change without notice

Function Table

Internal Counter	Address	Address Input D_3 (A_3)	D_2 (A_2)	D_1 (A_1)	D_0 (A_0)	Address Output D_3	D_2	D_1	D_0	Count Value	Remarks
S_1	0	L	L	L	L	*	*	*	*	0 ~ 9	
S_{10}	1	L	L	L	H		*	*	*	0 ~ 5	
MI_1	2	L	L	H	L	*	*	*	*	0 ~ 9	
MI_{10}	3	L	L	H	H		*	*	*	0 ~ 5	
H_1	4	L	H	L	L	*	*	*	*	0 ~ 9	
H_{10}	5	L	H	L	H	*1	*	*	*	0 ~ 1 0 ~ 2	D2:H for p.m., L for a.m., D3:H for 24-hour clock, L for 12-hour clock. When D3 H is written, the D2 bit is reset inside the IC and remains constantly at L.
W	6	L	H	H	L		*	*	*	0 ~ 6	
D_1	7	L	H	H	H	*	*	*	*	0 ~ 9	
D_{10}	8	H	L	L	L	*2	*2	*	*	0 ~ 3	D2 and D3 in the D10line are for leap year selection.
MO_1	9	H	L	L	H	*	*	*	*	0 ~ 9	
MO_{10}	A	H	L	H	L				*	0 ~ 1	
Y_1	B	H	L	H	H	*	*	*	*	0 ~ 9	
Y_{10}	C	H	H	L	L	*	*	*	*	0 ~ 9	
	D	H	H	L	H						These selections are for resetting the 5-stage and the BUSY circuit after the $1/2^{15}$ frequency stage. Resetting is activated by latching this code on to the address latch and setting the WRITE input to H.
	EIF	H	H	H	L/H	$\frac{1}{3600}$ Hz	$\frac{1}{60}$ Hz	1 Hz	1024 Hz		These selections are for obtaining standard signals. By latching this code on to the address latch and setting READ to H, the standard signals will be output at D_0~D_3.

Calendar	D_3	D_2	Remainder when divided years by 4
Western	L	L	0
Japanese	L	H	3
	H	L	2
	H	H	1

Note 1. The blank spaces in the data input/output columns indicate that there are no bits. When READ is performed, the L level is output. When WRITE is performed nothing will be stored in the memory because thre are no bits.

Note 2: The bit indicated by the symbol *1 is for selecting the 12hr/24hr clock and those indicated by *2 are for leap year selection. READ and WRITE are possible with all three bits.

Note 3: For address input, send a signal to the D_0~D_3 bus line, then input ADDRESS WRITE. The ADDRESS data will be latched on to the address latch.

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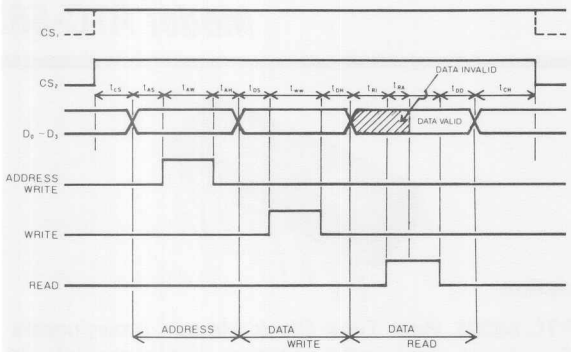
Write & Read Timing



(Ta=25°C V_{DD} = 5V ±5%)

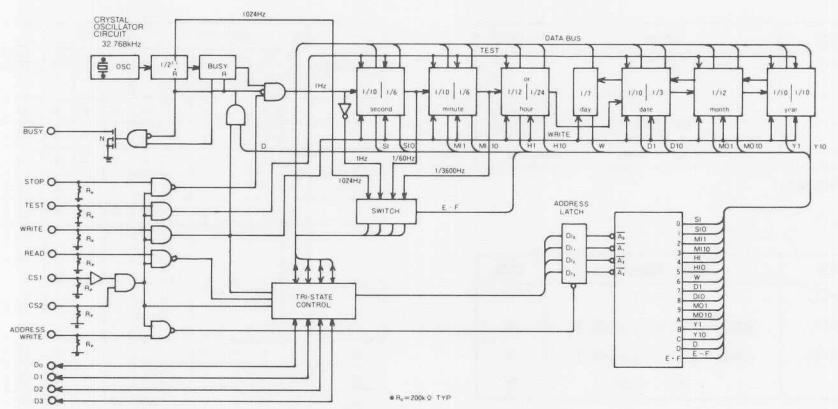
Item	Symbol	MIN	TYP	MAX	Units
CS set-up time	t_{CS}	0	—	—	μS
Address set-up time	t_{AS}	0	—	—	μS
Address write pulse range	t_{AW}	0.5	—	—	μS
Address hold time	t_{AH}	0.1	—	—	μS
Data set-up time	t_{DS}	0	—	—	μS
Write pulse range	t_{WW}	2	—	—	μS
Data hold time	t_{DH}	0	—	—	μS
Read inhibit time	t_{RI}	0	—	—	μS
Read access time	t_{RA}	—	—	*	μS
Read delay time	t_{DD}	—	—	1	μS
CS hold time	t_{CH}	0	—	—	μS

* $t_{RA} = 1\mu S + CR\ln\left(\frac{V_{DD}}{V_{DD}-V_H}\right)$

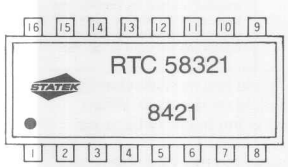
C: Data line wiring capacity
R: Pull-up resistance value
V_H: "H" input voltage of the IC connected to the data line
In: Natural logarithms

Specifications subject to change without notice.

Circuit Diagram



Pin Connections



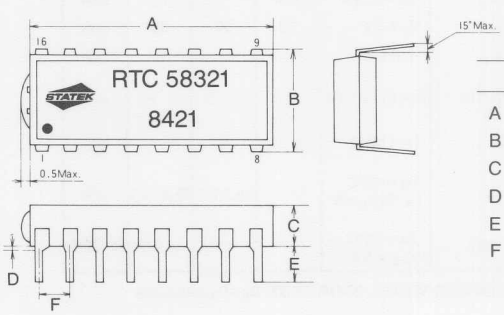
(Top View)

(Top View)

1. CS_2	16. V_{DD}
2. WRITE	15. NC
3. READ	14. NC
4. D_0	13. CS_1
5. D_1	12. TEST
6. D_2	11. STOP
7. D_3	10. $\overline{BUSY}$
8. V_{SS}	9. ADDRESS WRITE

NC: Do not connect externally.

Package Dimensions



	INCHES	MM
A	0.787	20
B	0.311	7.9
C	0.141	3.6
D	0.004	0.1
E	0.122	3.1
F	0.100	2.54

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